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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,677	02/01/2002	Robert J. Devins	BUR920010098	3095

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EXAMINER	
ALHIJA, SAIF A	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/683,677	DEVINS ET AL.	
	Examiner	Art Unit	
	Saif A. Alhija	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,5,7,16,17,19,21,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2, 3, 5, 7, 16, 17, 19, 21, and 31-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2, 3, 5, 7, 16, 17, 19, 21, and 31-32 have been presented for examination.

Claims 1, 2, 4, 6, 8-15, 18, 20, 22-30, and 33-36 have been cancelled.

Response to Arguments

2. Applicant's arguments with respect to claims 2, 3, 5, 7, 16, 17, 19, 21, and 31-32 have been considered but are moot in view of the new ground(s) of rejection.

i) Applicant's amendment has necessitated the new ground(s) of rejection presented in this Office action.

ii) Following Applicants amendment the objection to claim 21 is withdrawn.

iii) Following Applicants amendment the 101 rejections are withdrawn.

iv) Following Applicants arguments as well as the interview conducted 16 May 2007 the 112 2nd rejections are withdrawn.

v) Examiner has cited particular sections in the references applied to the claims for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

vi) The Examiner respectfully requests, in the event the Applicants choose to amend or add new claims, that such claims and their limitations be directly mapped to the specification, which provides support for the subject matter. This will assist in expediting compact prosecution.

vii) Further, the Examiner respectfully encourages Applicants to direct the specificity of their response with regards to this office action to the broadest reasonable interpretation of the claims as presented. This will avoid issues that would delay prosecution such as limitations not explicitly presented in the claims, intended use statements that carry no patentable weight, mere allegations of patentability, and novelty that is not clearly expressed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claim(s) 2, 3, 5, 7, 16, 17, 19, 21, and 31-32 are rejected** under 35 U.S.C. 102(b) as being clearly anticipated by **Blaner et al. "An embedded PowerPC SOC for Test and Measurement Applications", IEEE 2000, hereafter Blaner**.

Regarding Claim 2:

The reference discloses the computer system of claim 31, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to a respective second external I/O driver model of said second external I/O driver models. **(Figure 2. Page 207, Section IV-D. Page 208, Section IV-E.)**

Regarding Claim 3:

The reference discloses The computer system of claim 31, wherein said simulated external memory mapped test device further includes a simulated address register. **(Page 208, Section IV-E.)**

Regarding Claim 5:

The reference discloses The computer system of claim 2, wherein each said simulated external memory mapped test device module further includes a simulated address register. **(Page 208, Section IV-E.)**

Regarding Claim 7:

The reference discloses The computer system of claim 31, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to a respective second external I/O driver model of said one or more second external I/O driver models; and executing said instructions causes the computer to perform the further following steps:

loading code representing an additional simulated external memory mapped test device module into said memory unit; **(Page 208, Section IV-E, "memory-mapped external device")**

said loading of said test case connecting one or more additional second external I/O driver models to said additional simulated external memory mapped test device by additional simulated I/O buses; **(Figure 2, OPB, UART, GPIB, etc)** and

said loading of said test case connecting each additional second external I/O driver model to a respective additional simulated I/O core by said simulated system bus, each additional simulated I/O core comprising said model of integrated circuit design. **(Page 207, Section IV, TOS)**

Regarding Claim 16:

The reference discloses The computer program product of claim 32, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory modules containing a portion of said simulated switch and connected to one of said simulated I/O driver models. **(Page 208, Section IV-E, "memory-mapped external device") (Page 207, Section IV, TOS) (Figure 3, Chip Exerciser)**

Regarding Claim 17:

The reference discloses The program product of claim 32, wherein said simulated external memory mapped test device includes a simulated address register; and executing said instructions, further causes said computer to connect said simulated switch to one second external I/O driver model of said one or more second

external I/O driver models using address information programmed into said simulated address register. **(Page 208, Section IV-E.)**

Regarding Claim 19:

The reference discloses The program product of claim 16, wherein each simulated external memory mapped test device includes a corresponding simulated address register; and executing said instructions, further causes said computer to connect each portion of said simulated switch to one second external I/O driver model of said one or more I/O driver models using address information programmed into its corresponding said simulated address register. **(Page 208, Section IV-E.)**

Regarding Claim 21:

The reference discloses The computer system of claim 31, wherein said one or more simulated I/O cores are each independently selected from the group consisting of a simulated 1394 I/O core, a simulated universal asynchronous receiver transmitter core, a simulated serial core, a simulated general purpose I/O core, and a direct memory access core. **(Figure 2)**

Regarding Claim 31:

The reference discloses A computer system comprising a processor and a computer-readable memory unit coupled to communicate with said processor, said memory unit containing instructions that when executed by the causes the computer to perform the following steps:

loading code representing said integrated circuit design into said memory unit, said integrated circuit design including simulated I/O cores, a simulated memory controller, a simulated I/O controller, a simulated bus system and a simulated processor, said simulated I/O cores and said simulated I/O controller connected to said simulated processor by said simulated system bus; **(Figure 2. Page 207, Section IV-D. Page 208, Section IV-E.)**

loading into said memory unit, code representing (i) an external memory model connected to a simulated external memory mapped test device and to said simulated memory controller, (ii) one or more first external I/O driver models connected between said simulated I/O cores and said simulated external memory mapped test device

and (iii) one or more second external I/O driver models connected between a simulated switch of said simulated external memory mapped test device and said I/O controller, said simulated switch programmably connectable to said one or more second external I/O driver models in response to computer-executable instructions in a test case all said connections of (i), (ii) and (iii) by corresponding simulated I/O buses; **(Page 208, Section IV-E, "memory-mapped external device") (Figure 2, OPB, UART, GPIB, etc)**

loading said test case, said test case comprising said list of computer- executable instructions for said simulated processor into said external memory model, said instructions describing selection of one or more simulated I/O cores and corresponding second external I/O models, allocation of pins of said I/O controller to selected simulated I/O cores and switch positions of said simulated switch to connect said corresponding second external I/O models to said I/O controller; **(Figure 3, Chip Exerciser)**

executing said test case and allocating and connecting I/O pins of said simulated I/O controller to one or more of said simulated I/O cores, and connecting said simulated external memory mapped test device to said simulated I/O controller through said corresponding second external I/O models; **(Page 207, Section IV, TOS)**

executing test stimuli of said test case on said simulated processor in order to generate data representing a response of said computer simulation model of said integrated circuit design to said test case; and **(Page 207, Section IV, TOS)**

outputting said data representing a response of said computer simulation model of said integrated circuit design to said test case to another computer readable media or another computer, (ii) display said data representing a response of said computer simulation model of said integrated circuit design on a computer screen, or both (i) and (ii). **(Page 207, Section IV, TOS)**

Regarding Claim 32:

The reference discloses A computer program product embodied on a computer readable medium comprising code that, when executed, causes a computer to perform the following:

load a model of said integrated circuit design into a memory of said computer, said integrated circuit design including simulated I/O cores including a simulated general purpose core, a simulated external memory controller, a simulated I/O controller, a simulated bus system and a simulated processor, said simulated I/O cores and said

simulated I/O controller connected to said simulated processor by said simulated system bus; **(Figure 2. Page 207, Section IV-D. Page 208, Section IV-E.)**

load into said memory unit, code representing (i) an external memory model connected to a simulated external memory mapped test device and to said simulated memory controller, (ii) one or more first external I/O driver models into said memory unit connected between said simulated I/O cores and said simulated external memory mapped test device and (iii) one or more second external I/O driver models connected between a simulated switch of said simulated external memory mapped test device and said I/O controller, said simulated switch programmably connectable to said one or more second external I/O driver models in response to computer-executable instructions in a test case, all said connections of (i), (ii) and (iii) by corresponding simulated I/O buses; **(Page 208, Section IV-E, "memory-mapped external device") (Figure 2, OPB, UART, GPIB, etc)**

load said test case, said test case comprising said list of computer-executable instructions for said simulated processor into said external memory model, said instructions describing selection of one or more simulated I/O cores and corresponding second external I/O models, allocation of pins of said I/O controller to selected simulated I/O cores and switch positions of said simulated switch to connect said corresponding second external I/O models to said I/O controller; **(Figure 3, Chip Exerciser)**

executing said test case and allocating and connecting I/O pins of said simulated I/O controller to one or more of said simulated I/O cores, and connecting said simulated external memory mapped test device to said simulated I/O controller through said corresponding second external I/O models; **(Page 207, Section IV, TOS) (Figure 3, Chip Exerciser)**

execute test stimuli of said test case on said simulated processor; **(Page 207, Section IV, TOS)**

generate data representing a response of said computer simulation model of said integrated circuit design to said test case; and **(Page 207, Section IV, TOS)**

(i) output said data representing a response of said computer simulation model of said integrated circuit design to said test case to another computer readable media or another computer, (ii) display said data representing a response of said computer simulation model of said integrated circuit design on a computer screen, or both (i) and (ii). **(Page 207, Section IV, TOS)**

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. All Claims are rejected.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAA

August 3, 2007

KAMINI SHAH
SUPERVISORY PATENT EXAMINER